

ABSTRACT

A clock input/output device has three-state inverters Iv1 to Iv3 and an inverter Iv4, which cooperate to make equal the on-state resistance through a supply-voltage-side (VDD-side) transistor and the on-state resistance through a ground-voltage-side (0-side) transistor so as to make equal to $VDD / 2$ the threshold voltage with reference to which the clock input/output device evaluates the input thereto to determine whether or not to change the state of the output thereof.